REMARKS/ARGUMENTS

Claim rejections
35 USC § 102

Claims 1-28 are rejected, under 35 USC 102(b), as being allegedly anticipated by Nemecek et al., U.S. Pat. No. 7,089,175 (hereinafter, Nemecek). The Applicant respectfully traverses the rejection in view of the following.

Independent Claim 1 recites a limitation whereby one or more clocks of the device under test are turned off, as claimed.

Nemecek discloses that a special sleep mode is implemented to assure that the emulation microcontroller does not interfere with the programming process for a microcontroller (see Nemecek, col. 3, lines 23-26). Nemecek further discloses that to enter the debug mode the In-Circuit Emulation pulls data0 line to a logic high and then releases the reset line while the data0 line remains at a logic high (see Nemecek, col. 16, lines 14-25). Moreover, Nemecek discloses that the In-Circuit Emulation system pulls the data0 line to a logic low and releases the reset line sequence of events causing the microcontroller to enter the sleep mode (see Nemecek, col. 16, lines 43-47). The In-Circuit Emulation then uses the data1 line as a programming clock line to clock data into the microcontroller in socket until all of the program lines have been clocked in after which the microcontroller halts and power is turned off to the pod,

completing the programming process (see Nemecek, col. 16, lines 48-50 and lines 63-67).

Nemecek fails to teach or suggest turning off one or more clock of the device under test, as claimed because Nemecek teaches entering a sleep mode by pulling data0 line to a logic low and clocking programming data using data1 line until the microcontroller is programmed. Accordingly, Nemecek neither teaches nor suggests the limitations of independent Claim 1 which is patentable, over Nemecek, under 35 U.S.C. 102(e). Dependent claims are patentable by virtue of their dependency.

Independent Claim 7 recites a limitation whereby upon receiving the first signal, discontinuing the sending of the clock signals from the device under test to the emulator device, as claimed.

As discussed above, Nemecek teaches entering a debug mode by pulling data0 line to a logic high and releasing the reset line while the data0 line is still at a logic high. Therefore, for similar rationale discussed above, Nemecek fails to teach or suggest a limitation whereby upon receiving the first signal, discontinuing the sending of the clock signals from the device under test to the emulator device, as claimed. Accordingly, Nemecek neither teaches nor suggests the limitations of independent Claim 7 which is patentable, over

Nemecek, under 35 U.S.C. 102(e). Dependent claims are patentable by virtue of their dependency.

Independent Claims 10, 16, 21 and 25 recite limitations similar to that of independent Claims 1 and 7 and are patentable, over Nemecek, under 35 U.S.C. 102(e), for similar reasons. Dependent claims are patentable by virtue of their dependency.

Moreover, Claims 4, 13 and 26 recite determining the number of clock signals and resuming execution in lock-step, as claimed. The Applicant does not understand Nemecek to teach or suggest determining the number of clock signals, as claimed. Furthermore, Nemecek teaches away from resuming execution in lock-step, as claimed because Nemecek specifically teaches that the microcontroller halts and that the power is turned off when the programming is completed (see Nemecek, col. 16, lines 63-67).

As such, allowance of Claims 1-28 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of rejections under 35 U.S.C. 102(e).

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-28 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-28 overcome the rejections of record and, therefore, allowance of Claims 1-28 is earnestly solicited.

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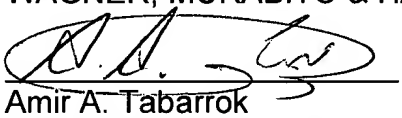
Respectfully submitted,
WAGNER, MURABITO & HAO LLP



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